

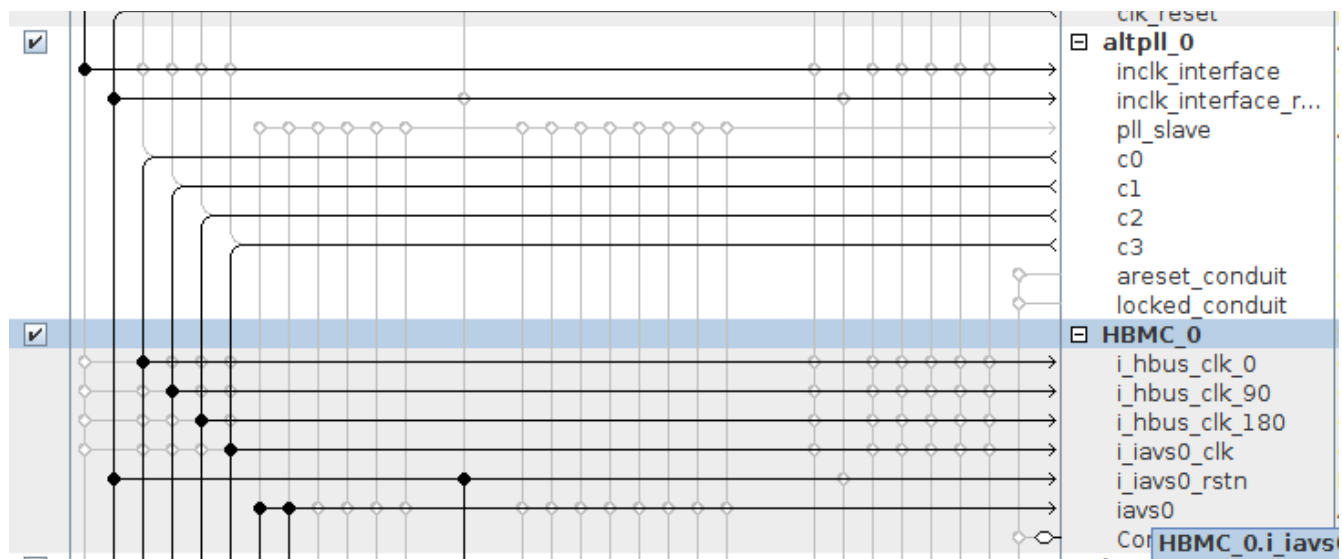
Application Note

Synaptic Labs' MBMC version 3.2.xx upgrade note

1.0 S/Labs' MBMC v3.1.x Original Configuration

With the external PLL configuration, S/Labs MBMC IP version 3.1.x requires 4 clocks :

- **i_hbus_clk_0** : clock driving the Hyperbus controller
- **i_hbus_clk_90** : clock for driving some Hyperbus I/O Signals. It operates at the same frequency as **i_hbus_clk_0** but is phase shifted 90 degrees
- **i_hbus_clk_180** : clock for driving some Hyperbus I/O Signals. It operates at the same frequency as **i_hbus_clk_0** but is phase shifted 180 degrees.
- **i_iavs0_clk** : clock driving the Avalon-MM interface. When S/Labs MBMC IP is configured to run at a single clock speed, this clock is connected to **i_hbus_clk_0** clock.

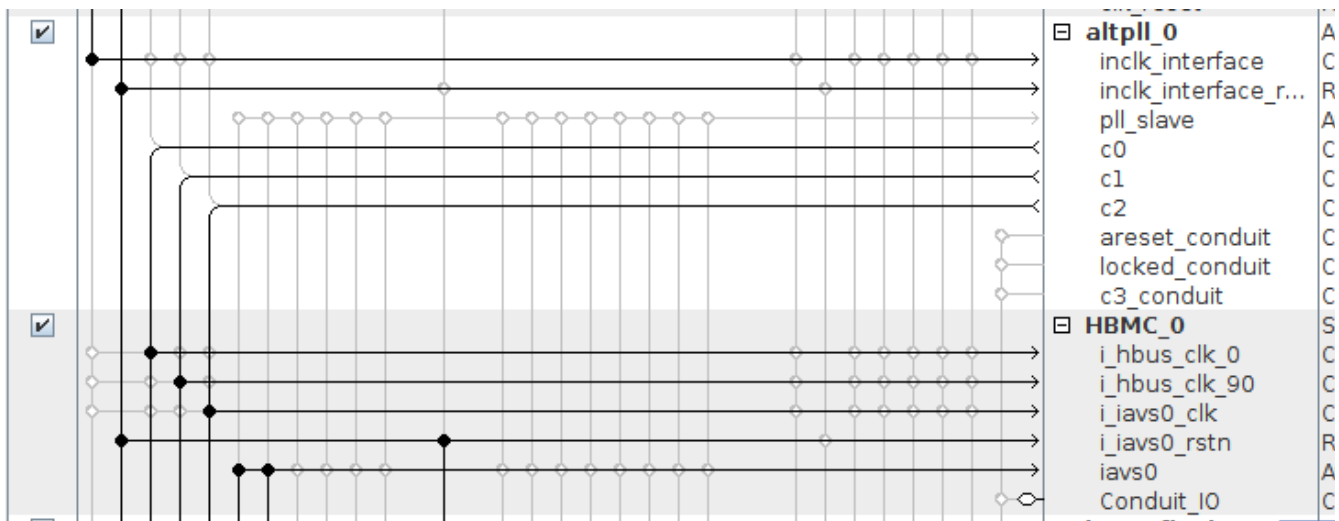


1.1 S/Labs' MBMC v3.2.x Updated Configuration

The update core does not require the **i_hbus_clk_180** clock, making the interface simpler. When updating the design, ensure to update the PLL configuration by removing the phase shifted 180 degrees clock.

With the external PLL configuration, S/Labs MBMC IP version 3.2.x requires only 3 clocks :

- **i_hbus_clk_0** : clock driving the Hyperbus controller
- **i_hbus_clk_90** : clock for driving some Hyperbus I/O Signals. It operates at the same frequency as **i_hbus_clk_0** but is phase shifted 90 degrees
- **i_iavs0_clk** : clock driving the Avalon-MM interface. When S/Labs MBMC IP is configured to run at a single clock speed, this clock is connected to **i_hbus_clk_0** clock.



1.2 Altera IO PLL Configuration on the **ARRIA 10** and **Cyclone 10 GX** FPGA

When configuring Altera's IO PLL , please ensure that

- Outclock0 is renamed to **clk_0**.
- Outclock1 is renamed to **clk_90** and phase shift is set to 90 degrees.s.
- Outclock2 is renamed to **clk_core** (Only needed when S/Labs' MBMC IP is configured with separate clocks on the Hyperbus channel and Avalon-MM channel)

Parameters System: niosll Path: altpll_0

Altera IOPLL
altera_iopll

outclk0

| | |
|----------------------|-----------|
| Clock Name: | clk_0 |
| Desired Frequency: | 100.0 MHz |
| Actual Frequency: | 100.0 |
| Phase Shift Units: | ps |
| Desired Phase Shift: | 0.0 ps |
| Actual phase shift: | 0.0 |
| Desired Duty Cycle: | 50.0 % |
| Actual duty cycle: | 50.0 |

Nearest Legal Values 0

outclk1

| | |
|----------------------|--------------|
| Clock Name: | clk_90 |
| Desired Frequency: | 100.0 MHz |
| Actual Frequency: | 100.0 |
| Phase Shift Units: | degrees |
| Desired Phase Shift: | 90.0 degrees |
| Actual Phase Shift: | 90.0 |
| Desired Duty Cycle: | 50.0 % |
| Actual duty cycle: | 50.0 |

Nearest Legal Values 1

outclk2

| | |
|----------------------|---------------|
| Clock Name: | clk_180 |
| Desired Frequency: | 100.0 MHz |
| Actual Frequency: | 100.0 |
| Phase Shift Units: | degrees |
| Desired Phase Shift: | 180.0 degrees |
| Actual Phase Shift: | 180.0 |
| Desired Duty Cycle: | 50.0 % |
| Actual duty cycle: | 50.0 |

Nearest Legal Values 2

Altera IOPLL
altera_iopll

outclk0

| | |
|----------------------|-----------|
| Clock Name: | clk_0 |
| Desired Frequency: | 150.0 MHz |
| Actual Frequency: | 150.0 |
| Phase Shift Units: | ps |
| Desired Phase Shift: | 0.0 ps |
| Actual phase shift: | 0.0 |
| Desired Duty Cycle: | 50.0 % |
| Actual duty cycle: | 50.0 |

Nearest Legal Values 0

outclk1

| | |
|----------------------|--------------|
| Clock Name: | clk_90 |
| Desired Frequency: | 150.0 MHz |
| Actual Frequency: | 150.0 |
| Phase Shift Units: | degrees |
| Desired Phase Shift: | 90.0 degrees |
| Actual Phase Shift: | 90.0 |
| Desired Duty Cycle: | 50.0 % |
| Actual duty cycle: | 50.0 |

Nearest Legal Values 1

outclk2

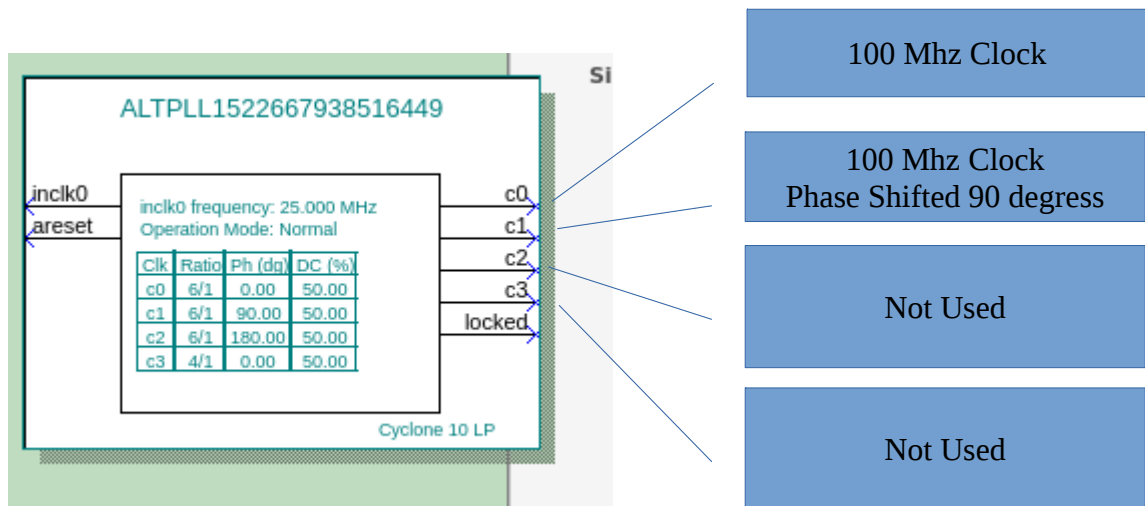
| | |
|----------------------|-----------|
| Clock Name: | clk_core |
| Desired Frequency: | 100.0 MHz |
| Actual Frequency: | 100.0 |
| Phase Shift Units: | ps |
| Desired Phase Shift: | 0.0 ps |

2.1 Option A – Same Clock for the Hyperbus memory channel and Avalon-MM channel.

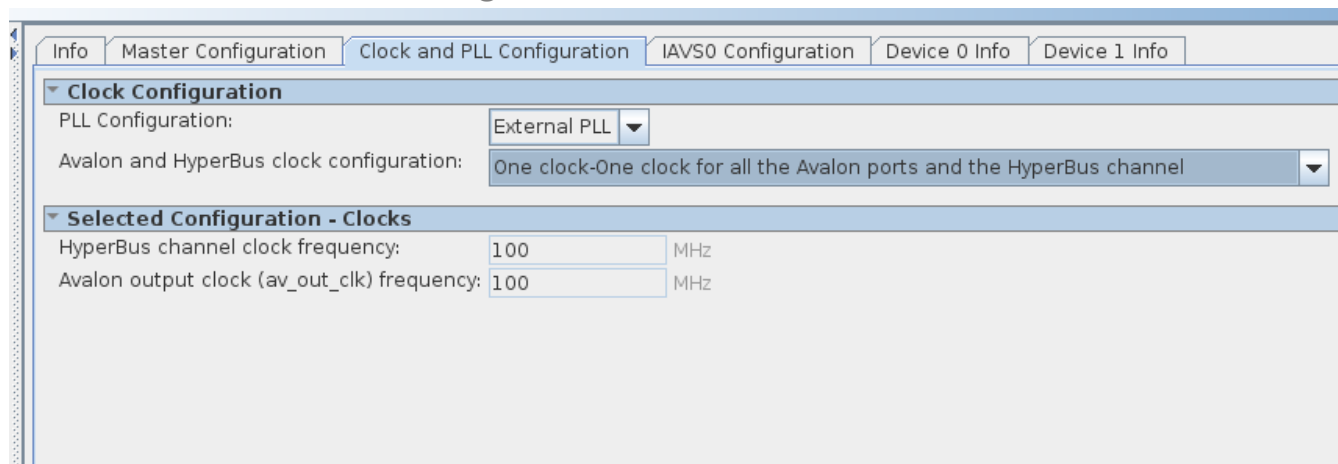
This configuration shows how to connect S/Labs' MBMC IP so that the Hyperbus memory channel operates at the same frequency as the Avalon-MM bus interface. The advantage of this configuration is lower circuit area.

2.1.1 Clocking (PLL) Wizard Configuration

The figure below shows a typical example of configuring the Clocking wizard . In this case, the clocks for the Hyperbus channel and Avalon-MM interface channels are all set to 100 Mhz.



2.1.2 S/Labs' MBMC Configuration

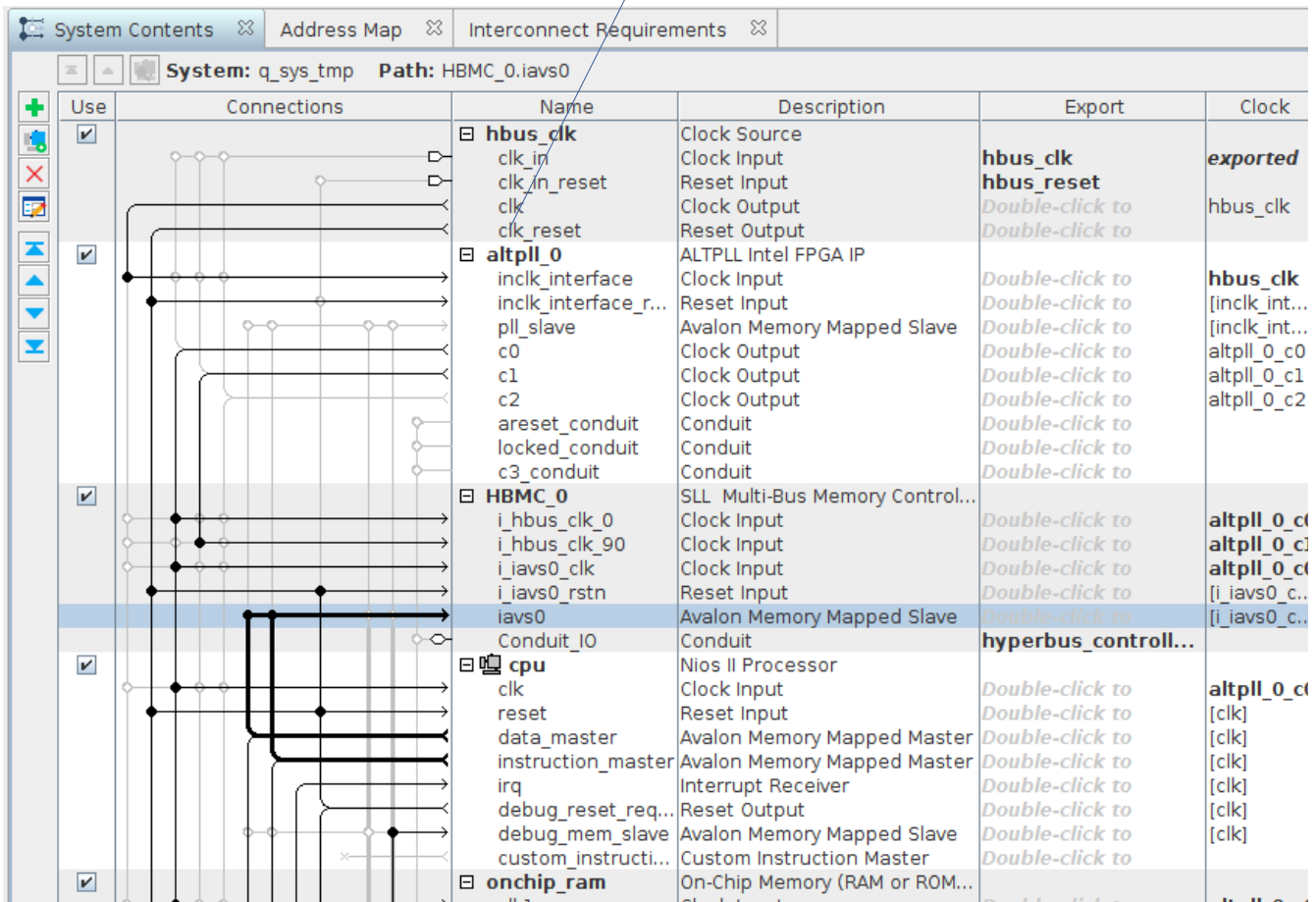


In this example, S/Labs' MBMC IP is configured with :

- AXI/Hyperbus Clock Dependency : **External PLL**
- AXI/Hyperbus Clock Dependency : **One clock**

2.1.3 S/Labs' MBMC wiring

Ensure that the PLL name is altpll_0



Altera PLL output clock 0 (c0)

- Connect to i_hbus_clk_0 and i_iavs0_clk on S/LABS MBMC IP
- Connect to other Avalon-MM slaves and masters clock sinks

Altera PLL output clock 1 (c1)

- Connect to i_hbus_clk_90 on S/LABS MBMC IP

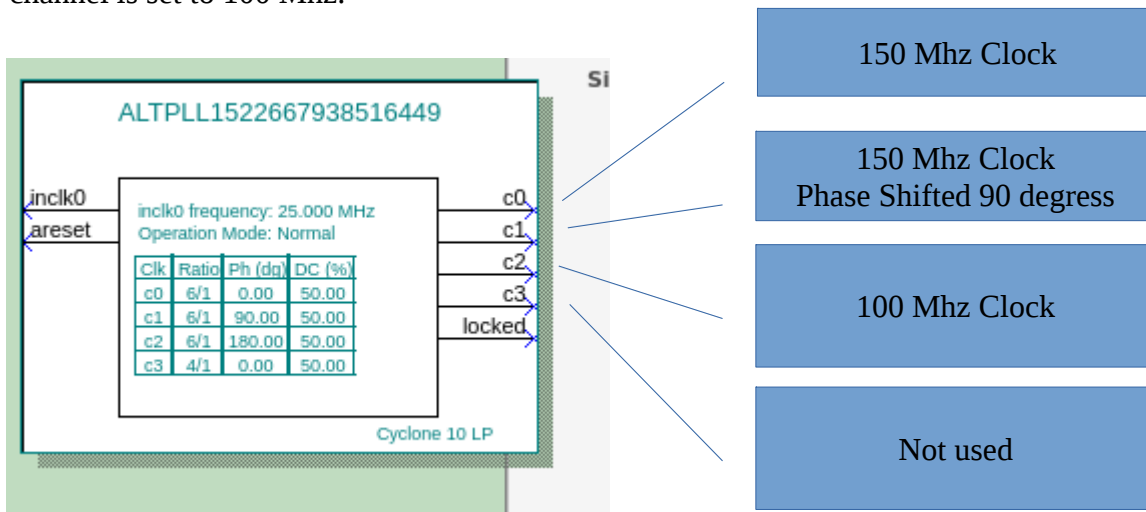
Note how i_hbus_clk_0 and i_iavs0_clk are connected to the same clock.

2.2 Option B – Different Clocks for the Hyperbus memory channel and AXI channel .

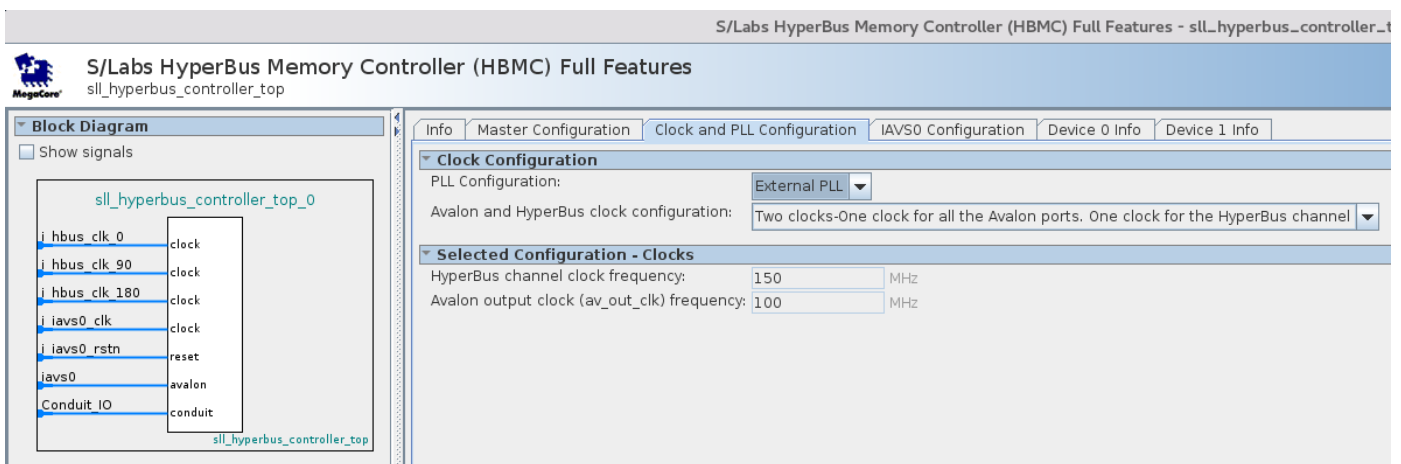
This configuration shows how to connect S/Labs' MBMC IP so the Hyperbus memory channel operates at a different clock frequency than the Avalon-MM bus interface.

2.2.1 Clocking Wizard Configuration

The figure below shows a typical example of configuring the Clocking wizard . In this case, the clocks for the Hyperbus channel are all set to 150 Mhz, while the clock for the Avalon-MM interface channel is set to 100 Mhz.



2.2.2 S/Labs' MBMC Configuration

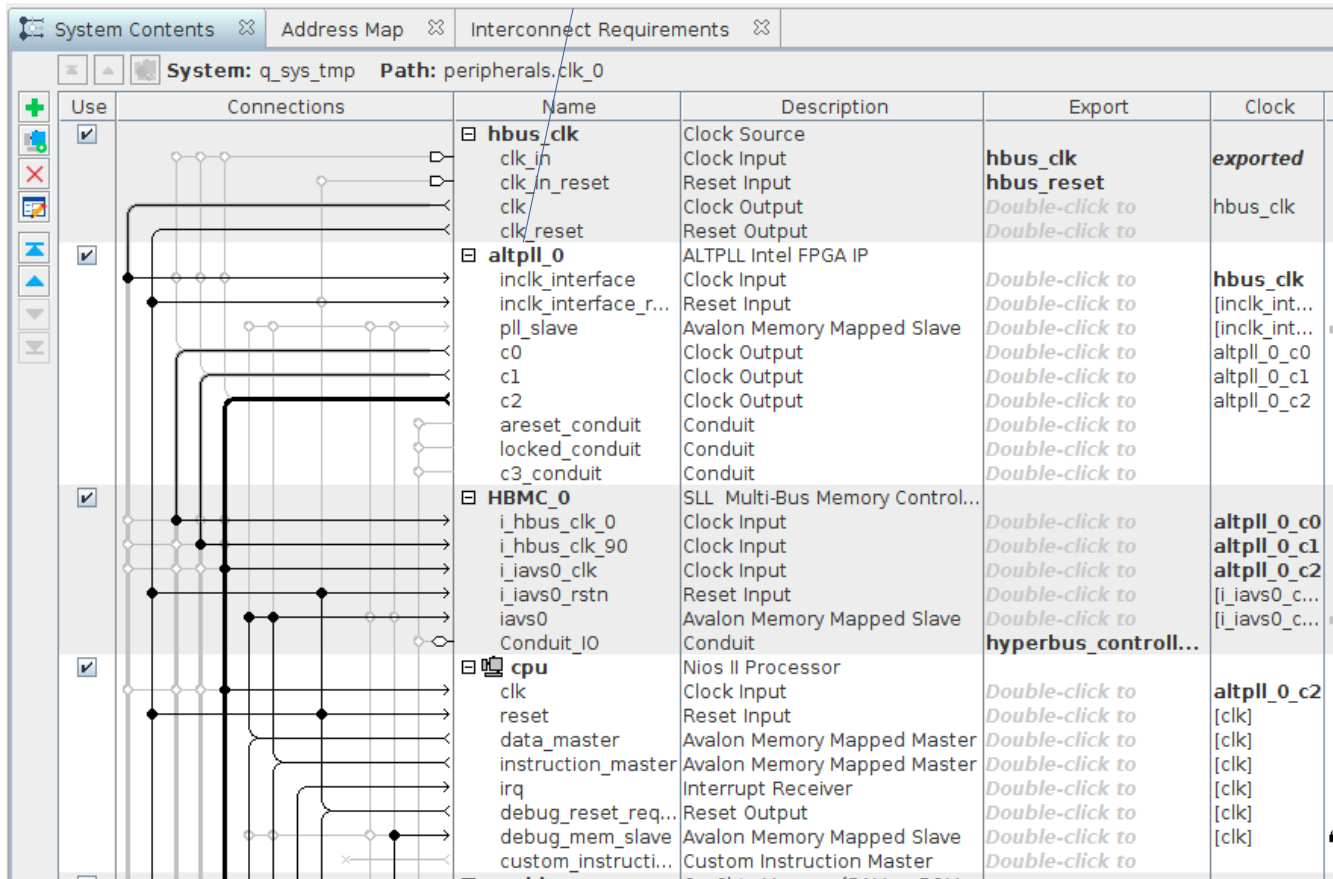


In this example, S/Labs' MBMC IP is configured with :

- AXI/Hyperbus Clock Dependency : **External PLL**
- AXI/Hyperbus Clock Dependency : **Two clocks**

2.1.3 S/Labs' MBMC wiring

Ensure that the PLL name is altpll_0



Altera PLL output clock 0 (c0)

- Connect to i_hbus_clk_0 on S/LABS MBMC IP

Altera PLL output clock 1 (c1)

- Connect to i_hbus_clk_90 on S/LABS MBMC IP

Altera PLL output clock 2 (c2)

- Connect to i_iavs0_clk on S/LABS MBMC IP
- Connect to other Avalon-MM slaves and masters clock sinks

Note how i_hbus_clk_0 and i_iavs0_clk are connected to a different clock.

Important :

Please note that S/Labs MBMC contains a script that sets timing constraints for the Hyperbus IO signals. For the external PLL configuration, this script assumes that in Qsys, Altera PLL's instance name is altpll_0.